REMARKS

In the last Office Action, the Examiner rejected claims 1, 2, 5, 6, 8, 9, 12, 13, 16 and 17 under 35 U.S.C. §102(b) as being anticipated by Liu (US 5,768,617). Additional art was cited of interest.

In accordance with the present response, the specification has been revised to correct informalities and bring it into better conformance with U.S. practice. Claims 1, 2, 5, 6, 8, 9, 12, 13, 16 and 17 have been amended to further patentably distinguish from the prior art of record, improve the wording, and bring the claims into better conformance with U.S. practice. New claims 18-23 have been added to provide a fuller scope of coverage. A new abstract which more clearly reflects the invention to which the amended and new claims are directed has been substituted for the original abstract.

Applicants request reconsideration of their application in light of the foregoing amendments and the following discussion.

The present invention is directed to a memory interface device and corresponding memory interface method and to a modem device having the memory interface device.

Conventional memory interface devices and methods have been unable to reduce loads on a memory readout unit (e.g., a CPU of a PC card) during memory write and read procedures. As a result, data written by the memory write unit and read by a

readout unit could not be processed with good efficiency, thereby degrading the processing speed of the memory interface device.

The present invention overcomes the drawbacks of the conventional art. Figs. 1-4 show an embodiment of a memory interface device 120 according to the present invention embodied in the claims. The memory interface device 120 controls memory access between a memory write unit 101 that writes data into a memory 100 and a memory readout unit 102 that reads the data from the memory 100. The memory write unit 101 is compliance with a memory write procedure in which each time data is written into a memory 100 by a predetermined unit amount, it is confirmed that readout of the data from the memory 100 has been completed, and then the next memory write procedure of the data into the memory 100 is performed.

The memory interface device 120 includes a write detection section 10 that detects the write of the predetermined unit amount of the data by the memory write unit 101 into the memory 100. A signal generation section 107 generates, upon detection of the writing of the predetermined unit amount of the data by the write detection section 10, a signal to notify the memory write unit 101 that the readout of the data from the memory 100 by the memory readout unit 102 has been completed. A data storage amount measurement section 104 measures an amount of the data stored in the memory 100 during the memory write procedures. A memory readout control section 111 generates an

interrupt signal with respect to the memory readout unit 102 when the stored data amount in the memory 100 reaches a predetermined readout start storage amount. A timer 108 counts a period in which writing of the predetermined unit amount of the data into the memory 100 by the memory write unit 101 is discontinued and outputs a timeout signal to the memory readout control section 111 when a value of the period count reaches a predetermined timer period. The memory readout control section 111 generates the interrupt signal with respect to the memory readout unit 102 even when the memory readout control section 111 receives the timeout signal output from the timer 108.

By the foregoing construction and corresponding functions, the present invention provides a memory interface device in which the number of interruptions during memory write and readout procedures is effectively reduced as compared to the conventional art. As a result, loads due to processing interruptions are reduced and data can be processed efficiently and integrally.

Applicants respectfully submit that amended claims 1, 2, 5, 6, 8, 9, 12, 13, 16 and 17 and newly added claims 18-23 patentably distinguish from the prior art of record.

Claims 1, 2, 5, 6, 8, 9, 12, 13, 16 and 17 were rejected under 35 U.S.C. §102(b) as being anticipated by Liu. Applicants respectfully traverse this rejection.

Amended independent claim 1 is directed to a memory interface device and requires write detection means, signal generation means, data storage amount measurement means, and memory readout control means and corresponding functions. According to the Examiner, Liu discloses write detection means (col. 11, lines 14-16), signal generation means (col. 12, lines 7-32), data storage amount measurement means (col. 11, lines 16-23), and memory readout control means (col. 11, lines 16-32) and corresponding functions.

While applicants disagree with the foregoing Examiner's interpretation of the disclosure in Liu, in order to advance prosecution independent claim 1 has been amended to further patentably distinguish from Liu by reciting a timer that counts a period in which writing of the predetermined unit amount of the data into the memory by the memory write unit is discontinued and that outputs a timeout signal to the memory readout control means when a value of the period count reaches a predetermined timer, the memory readout control means generating the interrupt signal with respect to the memory readout unit even when the memory readout control means receives the timeout signal output from the timer. Independent claims 2 and 8 have been similarly amended. The specific timer and corresponding functions and functional relationship with the memory readout control means recited in amended independent claims 1, 2 and 8 is not disclosed or described by Liu.

Amended independent claims 5 and 12 are directed to a memory interface method and require the steps of counting a period in which writing of the predetermined unit amount of the data is discontinued and generating the interrupt signal with respect to the memory readout unit when a value of the period count reaches a predetermined timer period. Amended independent claims 16 and 17 are directed to a modem device and require counting means for counting a period in which writing of the predetermined unit amount of the data into the memory is discontinued and for outputting a timeout signal to the memory readout control means when a predetermined value of the period count is reached, the memory readout control means generating the interrupt signal with respect to the memory readout unit even when the memory readout control means receives the timeout signal. No corresponding structural combination and combination of steps are disclosed or described by Liu as set forth above for amended independent claims 1, 2 and 8.

Therefore Liu cannot anticipate amended independent claims 1, 2, 5, 8, 12, 16 and 17. Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), citing Jamesbury Corp. v. Litton Industrial Products Inc., 225 USPQ 253, 256 (Fed. Cir. 1985) (The identical invention must be shown in as complete detail in the reference as contained in the claim.) Furthermore, Liu does not suggest the claimed subject matter and, therefore,

would not have motivated one skilled in the art to modify Liu's system and method to arrive at the claimed invention.

Claims 6, 9 and 13 depend on and contain all of the limitations of amended independent claims 5, 8 and 12, respectively, and, therefore, distinguish from Liu at least in the same manner as amended independent claims 5, 8 and 12.

In view of the foregoing, applicants respectfully request that the rejection of claims 1, 2, 5, 6, 8, 9, 12, 13, 16 and 17 under 35 U.S.C. §102(b) as being anticipated by Liu be withdrawn.

Applicants respectfully submit that new claims 18-23 also patentably distinguish from the prior art of record.

New claims 18-23 depend on and contain all of the limitations of amended independent claims 1, 2, 8, 9, 12 and 13, respectively, and, therefore, distinguish from the prior art of record at least in the same manner as set forth above for claims 1, 2, 8, 9, 12 and 13.

Claim of Priority and Retrieval of Priority Document

Applicants respectfully request that the Examiner acknowledge in the next PTO communication applicants' claim for foreign priority submitted with the filing of the application on November 30, 2006 and the retrieval by the PTO of the priority document from the JPO (Japanese Patent Office).

In view of the foregoing, favorable reconsideration and passage of the application to issue are most respectfully requested. In the event the Examiner determines that something further need be done to place the application in allowable form, it is respectfully requested that the Examiner telephone the undersigned attorney at the below-listed number whereupon any outstanding matter will be promptly attended to.

Respectfully submitted,

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JULY 10, 2009
Date